AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. – 18. (Canceled)

19. (New) A semiconductor memory device comprising:

a first and a second bit line;

a first word line; and

a memory cell having a first inverter including a first N-channel MOS transistor and a first P-channel MOS transistor, a second inverter including a second N-channel MOS transistor and a second P-channel MOS transistor with an input terminal being coupled to an output terminal of said first inverter and with an output terminal being coupled to an input terminal of said first inverter, a third N-channel MOS transistor having a source/drain path coupled between the output terminal of said first inverter and the first bit line, and a fourth N-channel MOS transistor having a source/drain path coupled between the output terminal of said second inverter and the second bit line;

wherein said first and third N-channel MOS transistors are formed in a first P-type well region,

wherein said second and fourth N-channel MOS transistors are formed in a second P-type well region,

wherein said first and second P-channel MOS transistors are formed in an N-type well region which is located between said first and second P-type well regions,

wherein said first P-type well region includes a first diffusion layer and said N-type well region includes second and third diffusion layers,

wherein an outer shape of said first diffusion layer, defined by an isolation layer which extends along substantially the entirety of each of the longitudinal sides of said first diffusion layer, is substantially linearly symmetric relative to a line extending in a first direction through said first P-type well region,

wherein a boundary of said first P-type well region and said N-type well region extends in said first direction,

wherein said input terminal of said first inverter is a first gate electrode commonly belonging to said first N-channel MOS transistor and said first P-channel NOS transistor,

wherein said input terminal of said second inverter is a second gate electrode commonly belonging to said second N-channel MOS transistor and said second P-channel MOS transistor,

wherein said first and second gate electrodes are connected to said second and third diffusion layers via silicide in first and second connect regions, respectively, and

wherein both of said first and second connect regions are formed in said N-type well region.

20. (New) The semiconductor memory device according to claim 19, wherein said outer shape of the diffusion layer in the first P-type well is an outer shape of a combination of rectangles.

21. (New) The semiconductor memory device according to claim 19, wherein said first bit line is located between a first power supply line and a first ground line,

wherein said second bit line is located between said first power supply line and a second ground line, and

wherein said first ground line is coupled to the source of said first N-channel MOS transistor and said second ground line is coupled to the source of said second N-channel MOS transistor.

22. (New) The semiconductor memory device according to claim 21, wherein said first bit line, said first power supply line, and said first and second ground lines are metal layers having a same level at a same metalization level.

23. (New) The semiconductor memory device according to claim 19, wherein the width of the gate of the first N-channel MOS transistor is larger than the width of the gate of the third N-channel MOS transistor.

24. (New) The semiconductor memory device according to claim 19, wherein said first word line lies in a metalization level between the substrate and the first and second bit lines.

25. (New) The semiconductor memory device according to claim 19, wherein a first polycrystalline silicon lead layer for use as the gate of said third N-channel MOS transistor and a second polycrystalline silicon lead layer for use as the

gate of said first P-channel MOS transistor and also as the gate of said first N-channel MOS transistor are disposed in parallel to each other,

wherein a third polycrystalline silicon lead layer for use as the gate of said fourth N-channel MOS transistor and a fourth polycrystalline silicon lead layer for use as the gate of said second N-channel MOS transistor and also as the gate of said second P-channel MOS transistor are disposed in parallel to each other, and

wherein the first and third polycrystalline silicon lead layers are connected via a contact to a second layer of a metal lead layer constituting said first word line.

26. (New) A semiconductor device comprising:

first and second inverters with an output of the first inverter being coupled to an input of the second inverter and an output of the second inverter being coupled to an input of the first inverter

a first switch connected to a connection node between an output of the first inverter and an input of the second inverter; and

a second switch connected to a connection node between an input of said first inverter and an output of said second inverter,

wherein said semiconductor device has an N-type well region and first and second P-type well regions disposed on opposite sides of said N-type well region,

wherein a diffusion layer formed in each of said N-type well region and said first and second P-type well regions is arranged in planar shape to have one of:

a shape consisting essentially of a single rectangle having long sides in an elongate direction of a boundary line of said N-type well region and said first and second P-type well regions; and

a shape resulting from a combination of a plurality of rectangles in the elongate direction of the boundary line of said N-type well region and said first and second P-well regions, the rectangles having long sides in said elongate direction,

wherein an input terminal of said first inverter is connected to said diffusion layer being formed in said N-type well region and being an output terminal of said second inverter, and said input terminal of said first inverter is connected to said diffusion layer being said output terminal of said second inverter via silicide in a first connect region being formed in said N-type well region, and

wherein an input terminal of said second inverter is connected to said diffusion layer being formed in said N-type well region and being an output terminal of said first inverter, and said input terminal of said second inverter is connected to said diffusion layer being said output terminal of said first inverter via silicide in a second connect region being formed in said N-type well region.

27. (New) The semiconductor device according to claim 26,

wherein the diffusion layer formed in said N-type well region or P-type well region has its planar shape of a combined form as resulting from a combination of a first rectangle having long sides in the elongate direction of boundary lines of said N-type well region and said first and second P-type well regions along with a short side of a first length and a second rectangle having long sides in the elongate direction of the boundary lines of said N-type well region and said first and second P-type well regions along with a short side of a second length, the combination being in the elongate direction of said boundary lines.